ABSTRACT

The invention provides, in an embodiment, a structure, method and means for generating clock phases, synchronized to the system clock, that to first order are independent of process parameters including drive current, parasitic resistance and parasitic capacitance. In one aspect, an apparatus is provided to generate an output phase at a predetermined time relative to an input clock signal and dependent on a logic phase width of the input clock signal. In another aspect, the apparatus includes similar circuit components with unequal units, the predetermined time is further dependent on the units ratio of the similar circuit components. In another aspect, the apparatus is cascaded with at least one reproduction of the apparatus, and configured to provide a multiple of the input clock signal. In another aspect, the apparatus is coupled in parallel with at least one reproduction of the apparatus, and configured to provide at least two output phases generated in parallel during the input clock signal.